HYBRIS

Enhanced Hybrid Storage Systems

Optimization of the HESS power conversion architecture

Workshop on energy storage and its crucial role in the energy transition with focus on hybrid solutions

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with collaboration from Oriol Esquius Project Engineer at IREC

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POWER SYSTEMS

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- 1st HYBRIS Workshop
- Horcynus Orca Foundation, 23rd June 2022

Framework

- *HYBRIS WP3 Task 3.3: Optimal electrical architecture of each BESS and the HESS (M9-M17)*

This task aims at achieving the optimal electrical and conversion architecture for hybrid electric storage systems (HESS).

An optimization problem is defined with a search space consisting of commercial passive and active electrical and electronic components.

The final target is to define an architecture for the HESS that would ensure the following:

- **Scalable** and **modular** power system for different ESS integration.
- Optimized **trade-off** among **efficiency**, **cost**, and **reliability**.

Work performed by IREC with the collaboration of CEA and the support from TOS and KEMI.

Hybrid Electric Storage System

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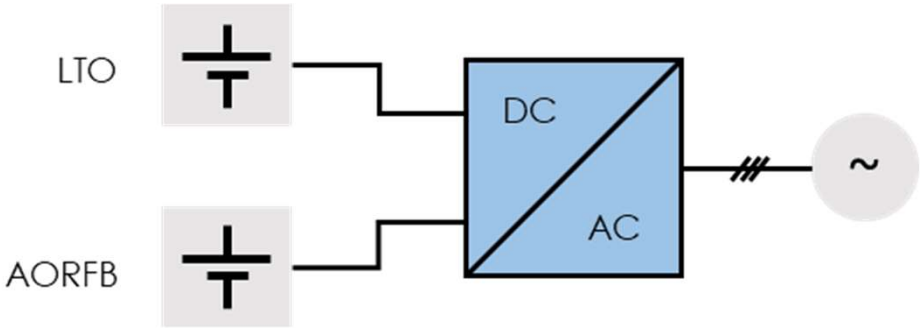
General scheme of the HESS

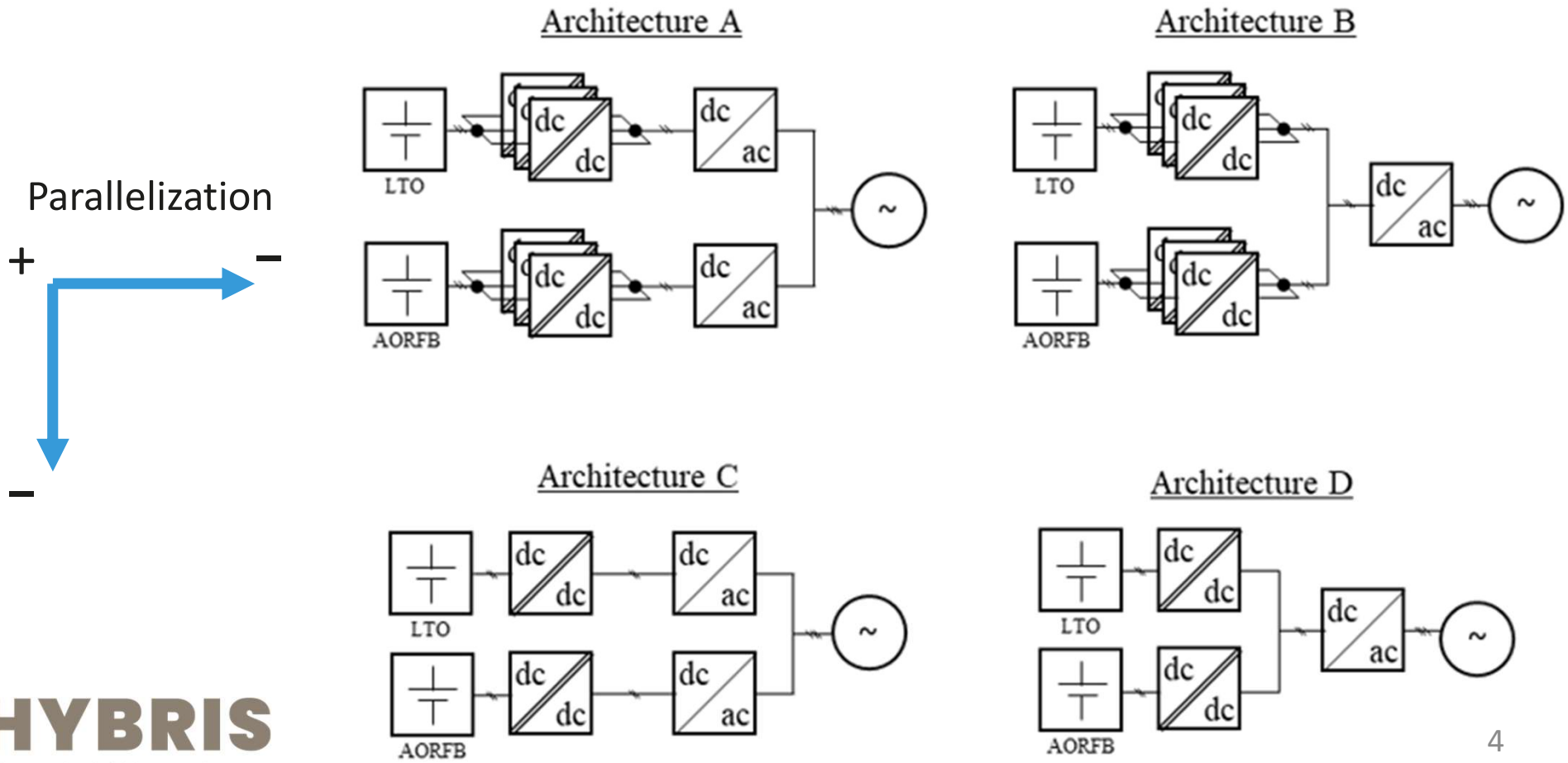


Power conversion system electrical ratings:

Port	dc nom. voltage	dc max. voltage	dc max. current	Nominal power	ac phase-to-phase nom. voltage	ac phase nom. current	ac nom. cos(φ)
dc (LTO)	330 V	390 V	200 A	50 kW	-	-	-
dc (AORFB)	50 V	70 V	165 A	9 kW	-	-	-
ac	-	-	-	59 kVA	400 V_{rms} ±10 %	85 A	1

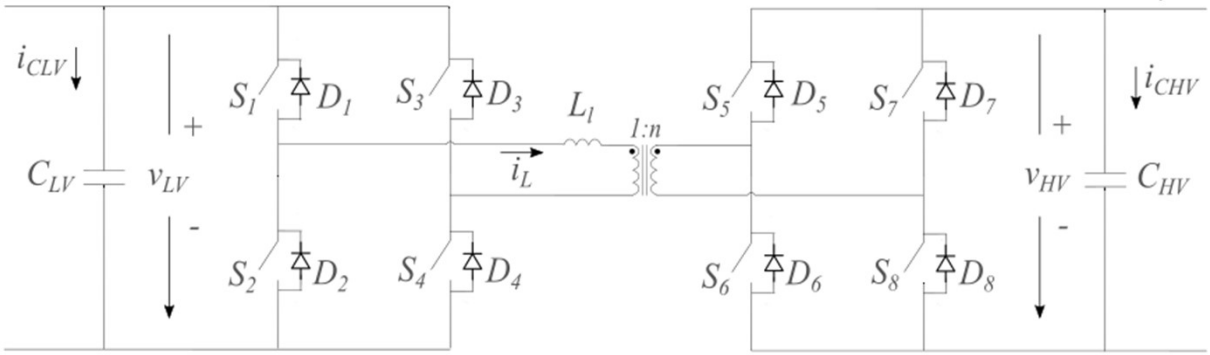
Explored power system architectures

- **Four conversion architectures** are explored, with different degrees of parallelization.

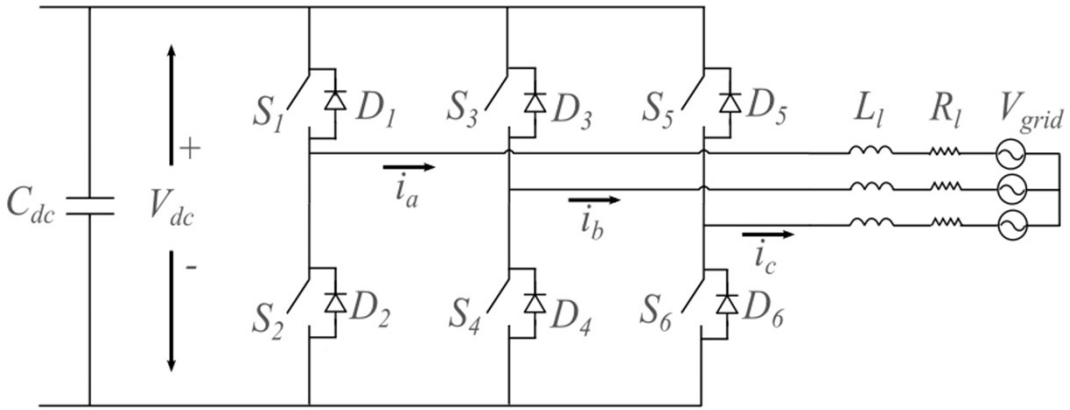


Power converter topologies

- **DC-DC modules**: Dual-active-bridge converter (DAB) employing conventional phase shift modulation.



- **DC-AC modules**: Three-phase inverter employing SPWM.



Multiobjective Optimization Problem

For each architecture ($x \in \{\mathrm{A}, \mathrm{B}, \mathrm{C}, \mathrm{D}\}$) a multiobjective optimization problem is defined.

Objective function:

$$G_{x,w}(\boldsymbol{y}) = W_{\zeta w} \cdot \zeta'_{x,w}(\boldsymbol{y}) + W_{\sigma w} \cdot \sigma'_{x,w}(\boldsymbol{y})$$

- $\zeta'_{x,w}$: Conversion losses (in p.u.).
- $\sigma'_{x,w}$: System capital and reliability cost (in p.u.).

To explore the cost-losses trade-off, weights $W_{\zeta w}$ and $W_{\sigma w}$ are used. Three different weight sets (WS) are defined:

- WS1: $\{W_{\zeta 1}, W_{\sigma 1}\} = \{0.5, 0.5\}$. Losses priority = Cost priority.
- WS2: $\{W_{\zeta 2}, W_{\sigma 2}\} = \{0.2\ 0.8\}$. Losses priority > Cost priority.
- WS3: $\{W_{\zeta 3}, W_{\sigma 3}\} = \{0.8\ 0.2\}$. Losses priority < Cost priority.

ζ – Conversion Losses Objective

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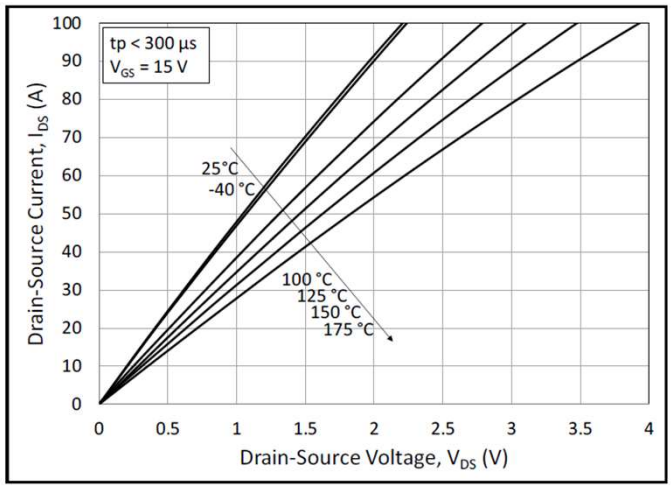
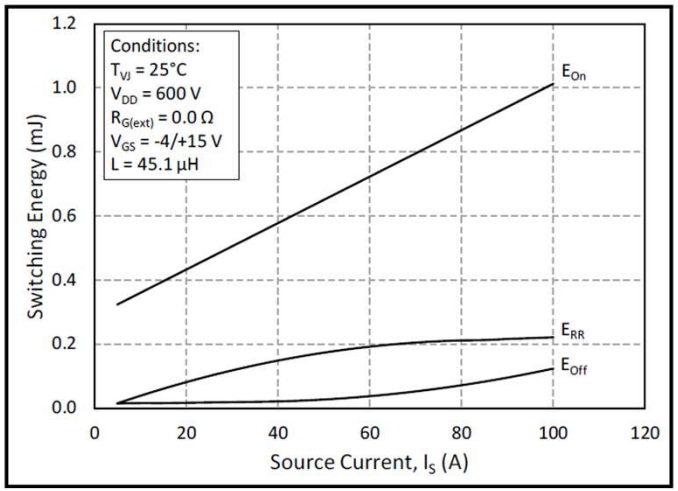
To compute the system losses we employ multiple converter component losses models.

- Semiconductor **conduction losses** and **switching losses**.
  - Modelled with linear equations from the devices datasheet data, taking into account junction temperature.





ζ – Conversion Losses Objective

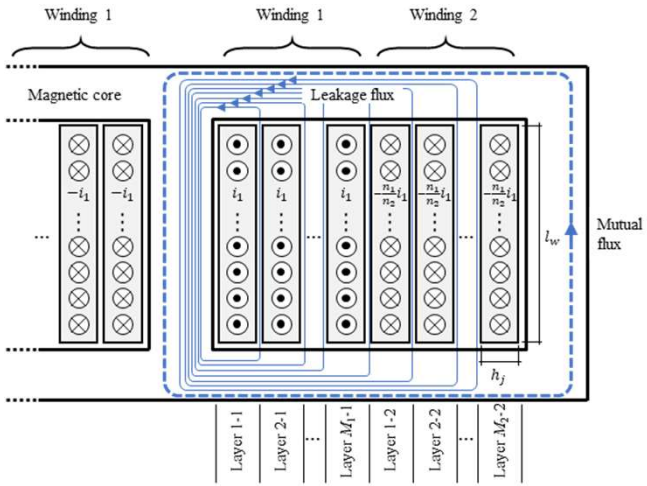
- Magnetic elements: DAB inductor + transformer and inverter filter inductors.
  - **Copper losses**: dc resistance and ac resistance (skin + proximity effect) in the winding conductors. From simplified Maxwell's equations [1].

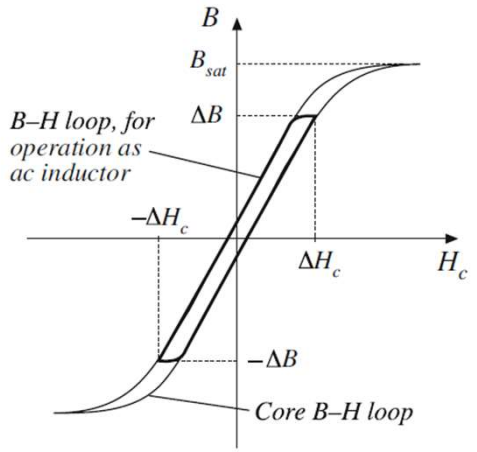
$$P_{\text{dc}} = \rho \cdot \frac{n_j \cdot MLT}{npw_j \cdot A_{\text{W},j}} \sum_{j=1}^{k} \cdot I_j^2 \quad | \quad P_{\text{ac},j} = I_{1,j}^2 \cdot R_{\text{dc},j} \cdot \varphi_j \cdot M_j \cdot \left[G_1(\varphi_j) + \frac{2}{3}\left(M_j^2 - 1\right)\left(G_1(\varphi_j) - 2G_2(\varphi_j)\right)\right]$$

  - **Core losses**: Polynomial regressions from core material datasheets.

$$P_{Fe} = K_{Fe0} \cdot f_1^{\xi} \cdot \Delta B^{\beta} \cdot N_c \cdot A_c \cdot l_m$$

  - **Capacitor losses**: derived from ESR: $P_{\text{cap}} = ESR \cdot I_c^2$ (ESR values obtained from the datasheets)





[1] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA, USA: Kluwer Academic Publishers, 2004.

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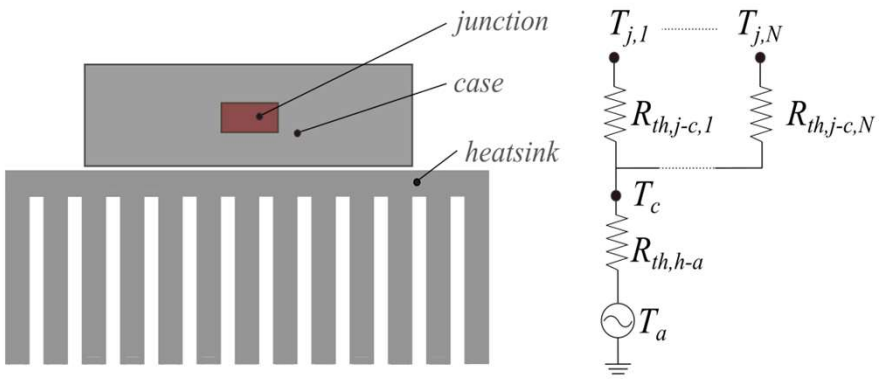
Thermal model

- We compute the component temperatures since:
  - **Semiconductor losses = $f(T_j)$**.
  - **Limit component temperatures** to the maximum specified by the manufacturer.
- Heat-dissipation thermal models:
  - **Semiconductors**: Power MOSFETs + body diode attached to heatsink (forced air cooling). Junction temperature (T_j) is computed.
  - **Magnetics**: Natural convection cooling. Uniform temperature is considered ($T_{\text{magnetic},k}$).
  - **Capacitors**: Free-standing capacitor with forced air cooling. Capacitor core temperature is computed ($T_{\text{cap},k}$).



- Semiconductors junction temperature

$$T_{j,n} = T_c + R_{th,\text{j–c},n} \cdot \left(P_{\text{cond},n} + P_{\text{sw},n}\right)$$

- Magnetic elements temeprature

$$T_{\text{magnetic},k} = T_{\text{amb}} + \left(\frac{P_{\text{core},k} + P_{\text{copper},k}}{10 \cdot S_{\text{magnetic},k}}\right)^{0.833}$$

- Capacitor core temperature

$$T_{\text{cap}} = T_{\text{amb},k} + \left(R_{th,\text{cap},0} + R_{th,\text{cap},1}(u_{\text{wind}})\right) \cdot P_{\text{cap}}$$

σ – Converter Cost Objective

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The system cost is divided in two parts:

- **Capital cost**: Sum of the components acquisition cost. Obtained from cost models [2], [3], [4].
  - Semiconductor cost = f(Chip area + Package)
  - Magnetics cost = f(Core weight + Copper weight + Labor cost)
  - Capacitors cost = f(Voltage rating + Capacitance rating)
  - Heatsink cost = f(HS volume + fixed cost)
  - Fan cost = f(Fan volume + fixed cost)
  - Auxiliary elements cost = f(#Gate drivers + #sensors)

Semiconductor chip area cost [€/mm^2]			
Voltage rating \ SC type	Si PiN Diode	Si MOSFET	SiC MOSFET
1200 V	$4.46 \cdot 10^{-2}$	-	$72 \cdot 10^{-2}$
600 V	$2.46 \cdot 10^{-2}$	$4.48 \cdot 10^{-2}$	$64.8 \cdot 10^{-2}$
100 V	-	$13.24 \cdot 10^{-2}$	-

Semiconductor package cost [€]			
Package type	TO-247-3	SOT 227	Module (variable)
Value	0.55	8.10	$0.52 \cdot A_{mod}$ - 4.8

Magnetic core cost [€/kg]			
Core material	Ferrite	Powder Core	Amorphous
Value	7.5	10.2	14.1

Winding cost [€/kg]			
Conductor type	Round	Litz	Foil
Value	10	10.2	20

[2] R. Burkart and J. W. Kolar, "Component cost models for multi-objective optimizations of switched-mode power converters," in 2013 IEEE Energy Conversion Congress and Exposition, Sep. 2013, pp. 2139–2146.
[3] R. M. Burkart and J. W. Kolar, "Comparative η-ρ-σ Pareto Optimization of Si and SiC Multi-Level Dual Active Bridge Topologies with Wide Input Voltage Range," IEEE Trans. Power Electron., pp. 1–1, 2016.
[4] R. M. Burkart and J. W. Kolar, "Comparative Life Cycle Cost Analysis of Si and SiC PV Converter Systems Based on Advanced η- ρ-σ Multiobjective Optimization Techniques," IEEE Transactions on Power Electronics, vol. 32, no. 6, pp. 4344–4358, Jun. 2017.

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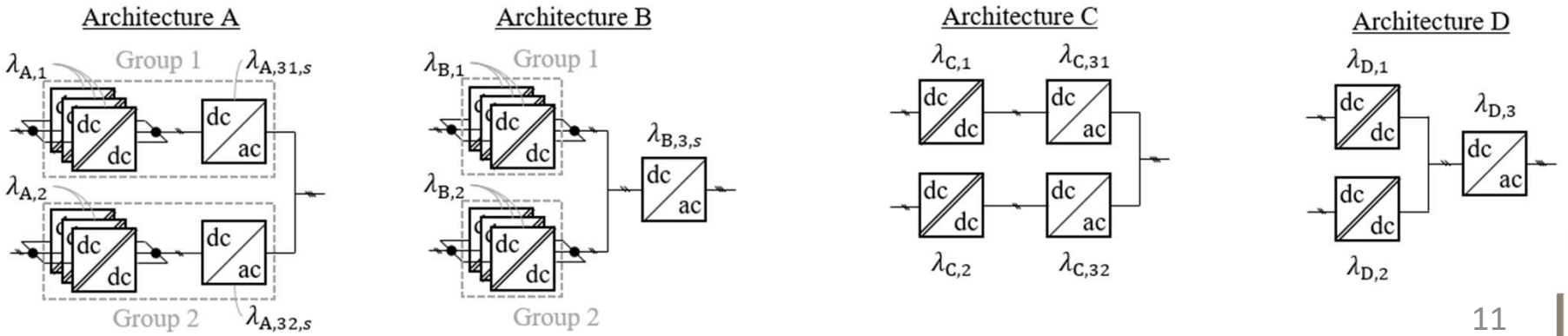
σ – Converter Cost Objective

- **Reliability cost** = Cost of reparation + Energy revenue lost
  - Reparation of failed power modules = f(Probability of modules failure + Reparation cost)
  - Revenue lost from partial/complete shutdown = f(Probability of modules failure + Power lost + Price of energy)
  - Computed for a 1-year period (demo-site testing period).
- **Reliability model**:
  - Based on Markov chains.
  - Allows computing the probability of failure of a power module.
  - Failure rate of the modules = f(Component temperatures & blocking voltages)
  - Architectures A & B can continue operation if one dc-dc module per group fails → Partial shutdown.
  - Architectures C & D must stop operation if any power module fails → Complete shutdown.



Optimization variables

$n_{\text{par,sw,DAB,bat},b}$	$L_{\text{HS,DAB,bat},b}$	$type_{\text{wire,L,DAB},b}$
$n_{\text{par,sw,DAB,grid},b}$	$L_{\text{HS,DAB,grid},b}$	$type_{\text{wire,Tx,DAB},b}$
$n_{\text{par,sw,inv},b}$	$L_{\text{HS,inv},b}$	$type_{\text{wire,L,inv},b}$
$type_{\text{sw,DAB,bat,LTO}}$	$n_{\text{par,cap,dclink},b}$	$model_{\text{wire,L,DAB},b}$
$model_{\text{sw,DAB,bat},b}$	$n_{\text{par,cap,bat},b}$	$model_{\text{wire,Tx,DAB},b}$
$model_{\text{sw,DAB,grid},b}$	$model_{\text{cap,bat},b}$	$model_{\text{wire,L,inv},b}$
$model_{\text{sw,inv},b}$	$model_{\text{cap,dclink},b}$	$n_{\text{t,L,DAB},b}$
V_{dc}	$n_{\text{core,L,DAB},b}$	$n_{\text{t,Tx,DAB,bat},b}$
$f_{\text{s,DAB},b}$	$n_{\text{core,Tx,DAB},b}$	$n_{\text{L,inv},b}$
$m_{f,b}$	$n_{\text{core,L,inv},b}$	$npw_{\text{L,DAB},b}$
$model_{\text{HS,DAB,bat},b}$	$model_{\text{core,L,DAB},b}$	$npw_{\text{Tx,DAB,bat},b}$
$model_{\text{HS,DAB,grid},b}$	$model_{\text{core,Tx,DAB},b}$	$npw_{\text{Tx,DAB,grid},b}$
$model_{\text{HS,inv},b}$	$model_{\text{core,L,inv},b}$	$npw_{\text{L,inv},b}$

- 76 optimization variables
- All variables are discrete

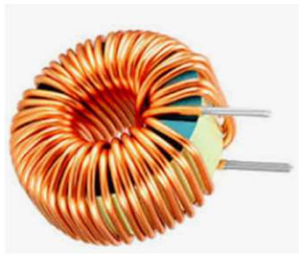
$b \in \{\text{LTO},\ \text{AORF}\}$

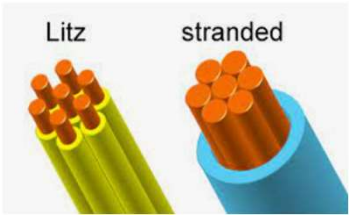
Design Space

Opt. variable	Design space
$n_{\mathrm{par,sw,DAB,bat},b}$	3, 4
$n_{\mathrm{par,sw,DAB,grid},b}$	Up to 2
$n_{\mathrm{par,sw,inv},b}$	Up to 2
$type_{\mathrm{sw,DAB,bat,LTO}}$	Discrete Si MOSFET, Discrete SiC MOSFET
$model_{\mathrm{sw,DAB,bat},b}$	LTO battery: - Si MOSFET: IRF100P218, IRF100P219, IPP023N10N5, IPP030N10N5, STF150N10F7, IPB120N10S4-03, SUP70090E, IPD122N10N3G, IPP126N10N3G - SiC MOSFET: UF3SC065007K4S AORF battery: - Si MOSFET: SiHG018N60E, SiHG026N60EF, IPZ60R017C7, IPW60R017C7, IPW60R018CFD7, IPW60R024CFD7, IPW60R024P7, IPZA60R024P7, IPW60R041P6, IPW60R060P7
$model_{\mathrm{sw,DAB,grid},b}$	SiC MOSFET modules: CAB006M12GM3, CAB008M12GM3
$model_{\mathrm{sw,inv},b}$	SiC MOSFET modules: CAB006M12GM3, CAB008M12GM3, CCB032M12FM3
V_{dc}	700 V, 750 V, 800 V
$f_{\mathrm{s,DAB},b}$	20 kHz, 24 kHz, …, 92 kHz, 96 kHz, 100 kHz
$m_{f,b}$	201, 219, 237, …, 687, 705, 723
$model_{\mathrm{HS,DAB,bat},b}$	From Advanced Thermal Solutions extrusion heat sinks catalogue: - ATS-EXL6, ATS-EXL59, ATS-EXL64, ATS-EXL66, ATS-EXL67, ATS-EXL75
$model_{\mathrm{HS,DAB,grid},b}$	
$model_{\mathrm{HS,inv},b}$	

Design Space

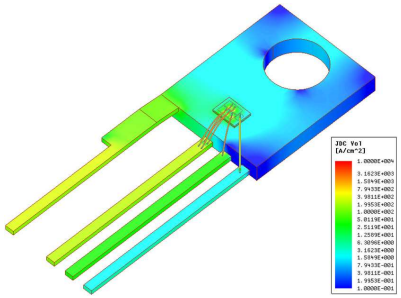
Opt. Variable	Design space
$model_{\text{cap,bat},b}$	From *Cornell Dubilier Electronics* film capacitors: *947D152K901DLRSN, 947C102K901DCHS, 947D112K102DLRSN, 947C641K102DBHS, 947C321K122DAHS, 944U101K122AC, 944U660K102AA*
$model_{\text{cap,dclink},b}$	
$n_{\text{core,L,DAB},b}$	1 to 5
$n_{\text{core,Tx,DAB},b}$	1 to 5
$n_{\text{core,L,inv},b}$	1 to 5
$model_{\text{core,L,DAB},b}$	From *Magnetics* cores catalogue: *0077169A7, 0077101A7, 0077336A7, 0059188A2, 0059909A2*
$model_{\text{core,Tx,DAB},b}$	From *Magnetics* cores catalogue: *00K114LE014, 0077164A7, 0077169A7, 0077101A7, 0077614A7, 0077336A7, 0077869A7, 0077740A7, 0077778A7*
$model_{\text{core,L,inv},b}$	From *Magnetics* and *TDK Electronics* cores catalogue: *E32/16/11* (Ferrite), *00K3112U090, 00K114LE014, 0077164A7, 0077169A7, 0077101A7, 0077614A7, 0077336A7, 0077869A7*
$type_{\text{wire,L,DAB},b}$	Round, Foil, Litz
$type_{\text{wire,Tx,DAB},b}$	Round, Foil, Litz
$type_{\text{wire,L,inv},b}$	Round, Foil, Litz
$model_{\text{wire,L,DAB},b}$	- Round wires: 2 AWG to 30 AWG - Litz wires: from ⌀0.04mm strand and 45 conductors per litz, to ⌀0.28mm strand and 1350 conductors per litz
$model_{\text{wire,Tx,DAB},b}$	
$model_{\text{wire,L,inv},b}$	
$n_{\text{t,L,DAB},b}$	Up to 25 turns
$n_{\text{t,Tx,DAB,bat},b}$	Up to 18 turns
$n_{\text{L,inv},b}$	Up to 30 turns

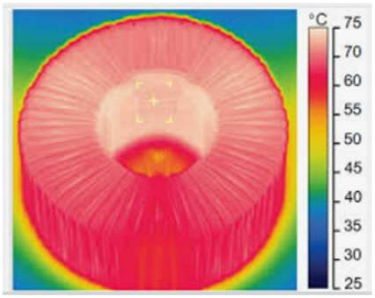


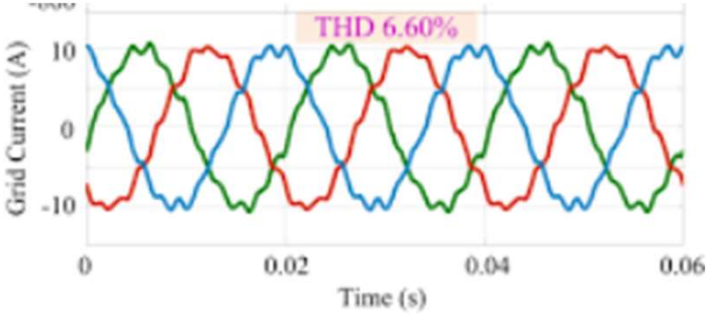


Constraints

- Semiconductors max. temperature < 120 ºC
- Magnetics max. temperature < 100 ºC
- Magnetics max. flux density < B_{sat} value from datasheet.
- Grid current THD < 10 %
- dc-link voltage ripple < 10 %
- …other constraints related to the converters modulation.







Optimization Problem Solving

$$\min_{\mathbf{y}} G_{x,w}(\mathbf{y}) = \mathrm{W}_{\zeta \mathrm{w}} \cdot \zeta'_{\mathrm{x,w}}(\mathbf{y}) + \mathrm{W}_{\sigma \mathrm{w}} \cdot \sigma'_{\mathrm{x,w}}(\mathbf{y})$$

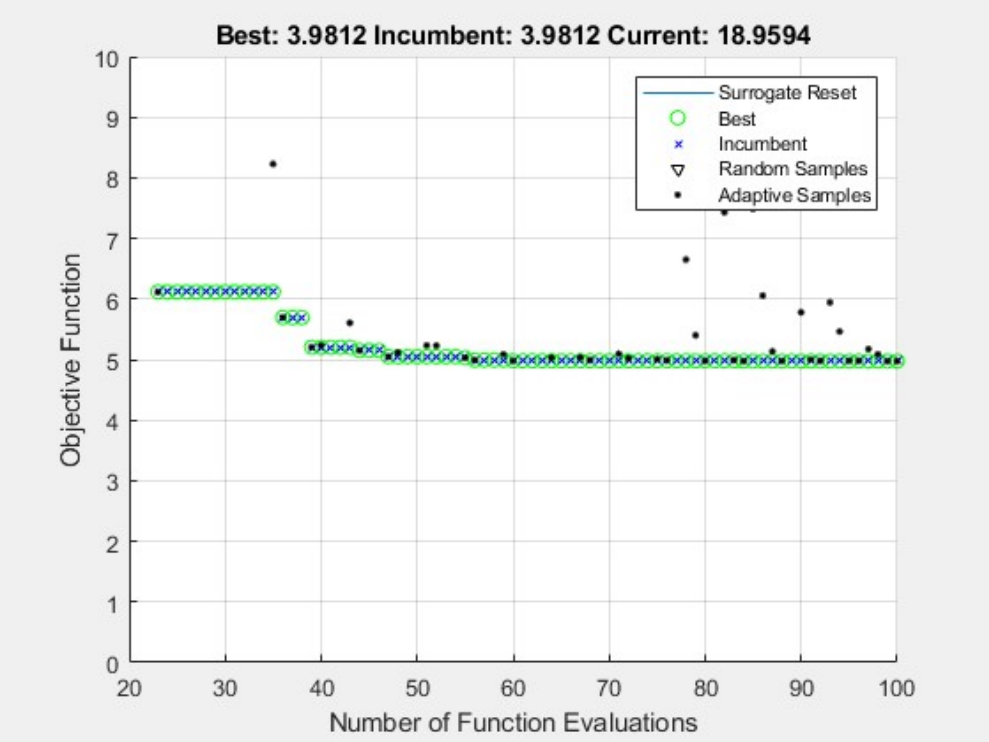
subject to constraints:

$$y_i \in \mathbb{Z}, \qquad i = 1, \ldots, 76$$

$$l_{\mathrm{b},i} \leq y_i \leq u_{\mathrm{b},i}, \qquad l_{\mathrm{b},i}, u_{\mathrm{b},i} \in \mathbb{Z}.$$

Solved with **MATLAB *Surrogate*** optimization algorithm.

Executed 6x times per architecture (x4) and weight set (x3) = 76 Executions.



Optimization results

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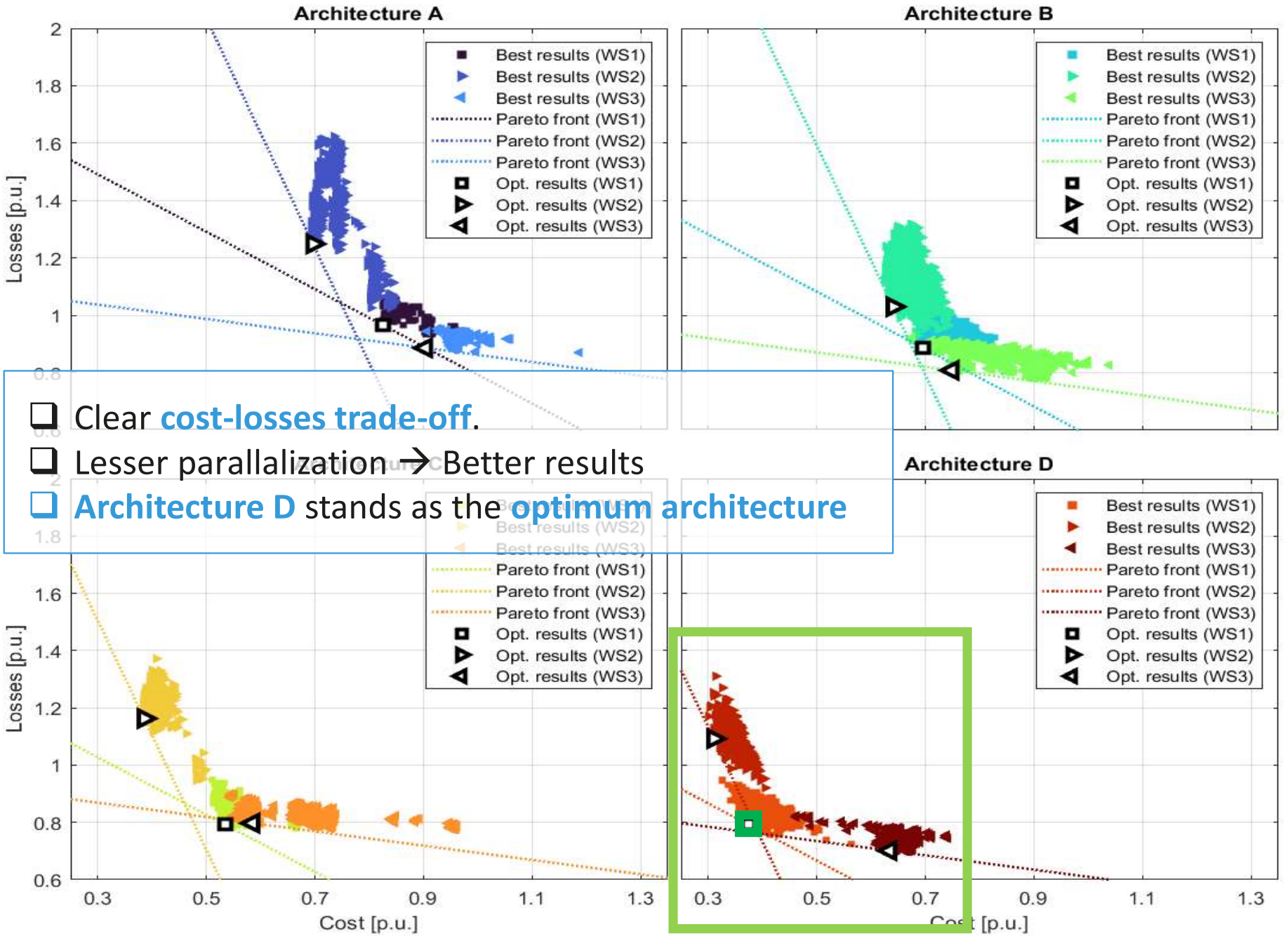

- Clear **cost-losses trade-off**.
- Lesser parallalization → Better results
- **Architecture D** stands as the **optimum architecture**

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Optimization results

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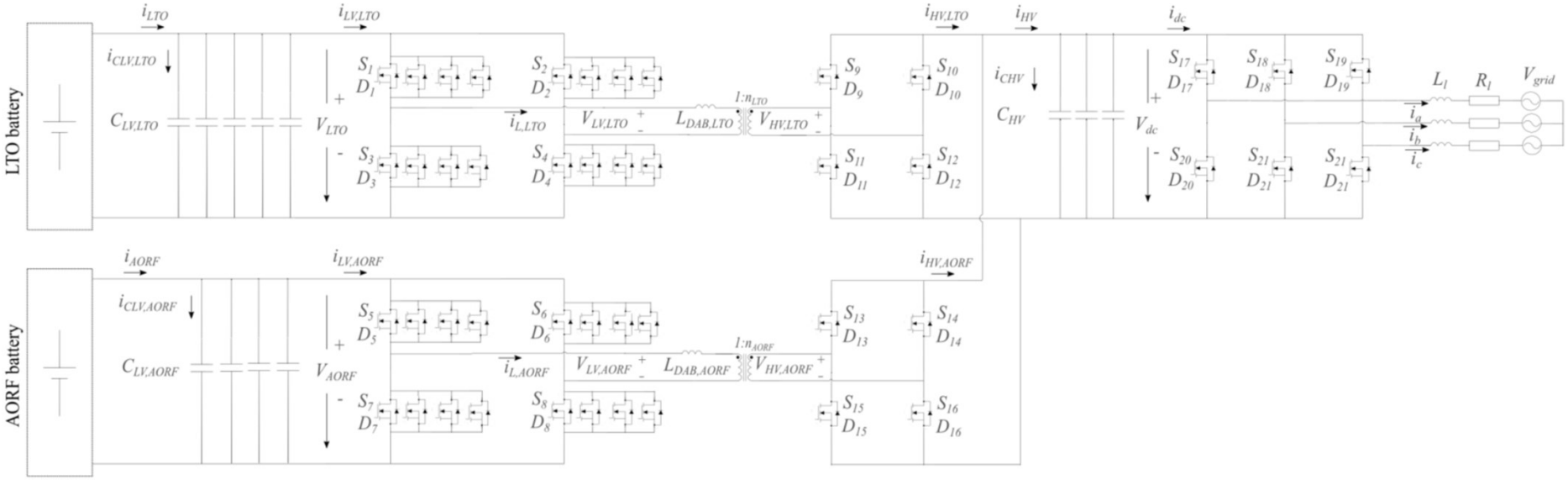
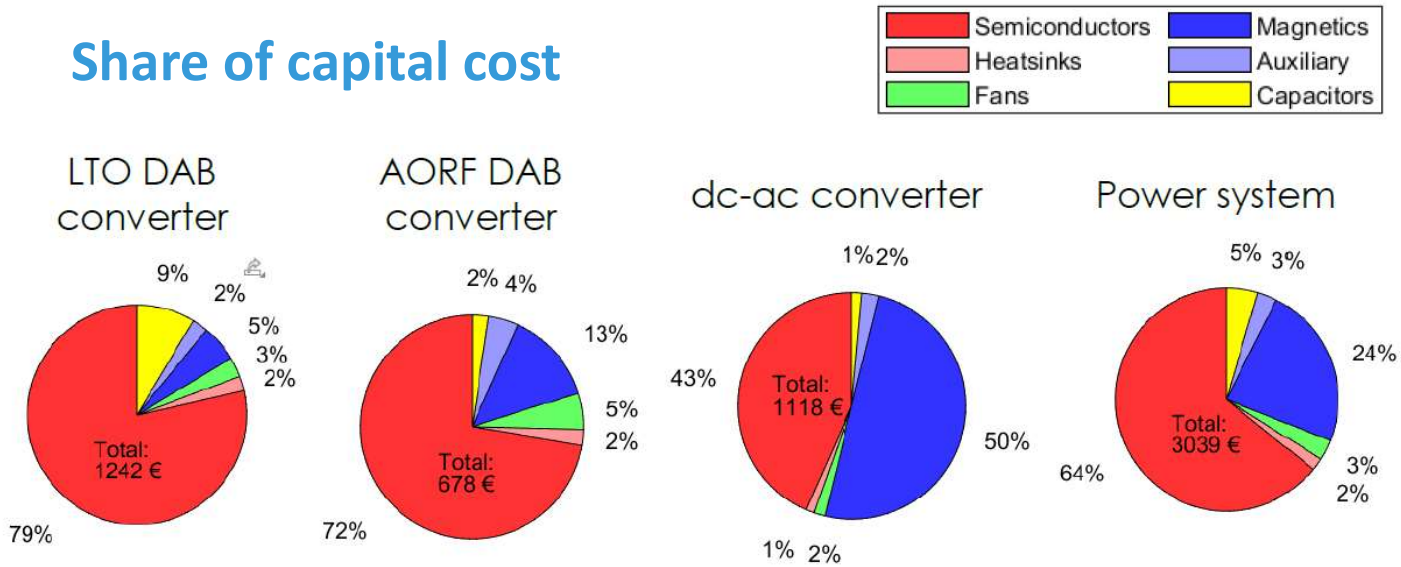
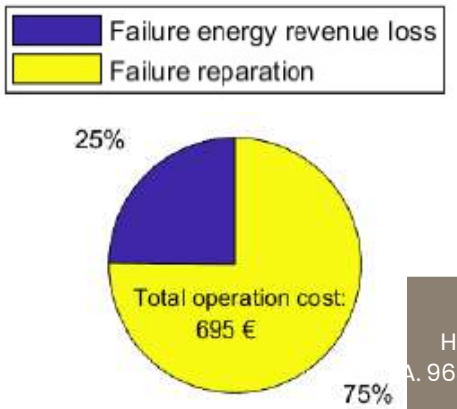
- **WS1 Arch. D** design is selected for its competitive cost-losses trade-off.



Share of capital cost



Share of reliability cost



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Conclusion

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We have developed an **Electronic Design Automation tool** with comprehensive and **multiphysics modelling** to:

- ❑ Obtain a set of power converter designs with **optimum performance** offering a **wide range** of **cost-losses trade-off**.
- ❑ The converter design are defined to the component level → **Ready-to-go for converter implementation**.

In HYBRIS context: Architectures with lower degree of parallelization offer the performance:

- ❑ However, if reliability cost is accounted for a longer period, these Architectures may not become cost competitive.

THANK YOU
FOR YOUR ATTENTION

This project has received funding
from the H2020 programme
under Grant Agreement No. 963652

Optimization results

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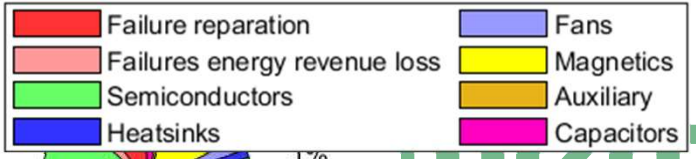
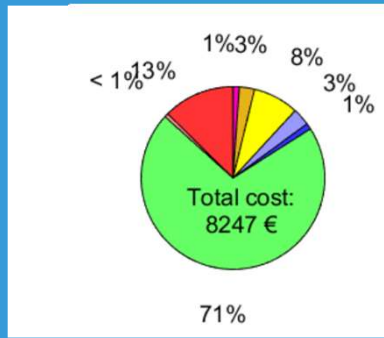
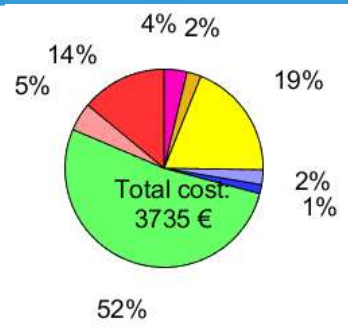
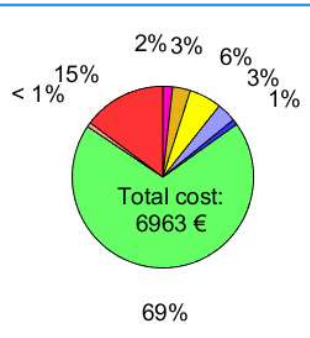
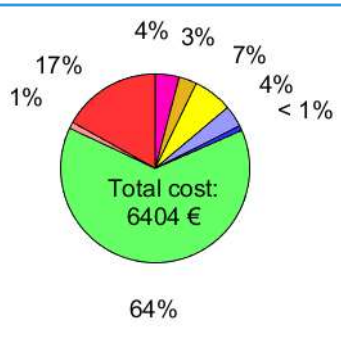
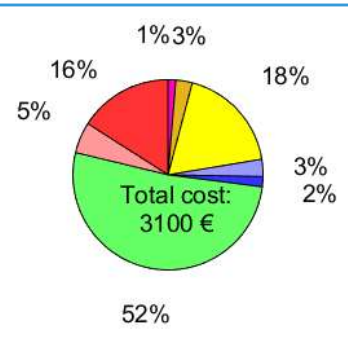
of the optimum solutions



	Architecture A	Architecture B	Architecture C	Architecture D
WS1				
WS2				
WS3